IN THE CLAIMS

1. (Previously Presented) A light-sensing pixel, having a p type doped region, in a CMOS image sensor, comprising:

a first doped charge collecting region buried within the p type doped region and configured to operate as a depleted potential well;

a first n+ type doped plug extending from near the surface of the image sensor to the first charge collecting region;

a second doped charge collecting region buried within the p type doped region, the second charge collecting region vertically separated from the first charge collecting region by the p type doped region and configured to operate as a depleted potential well;

a second n+ type doped plug extending from near the surface of the image sensor to the second charge collecting region;

a first extension with n+ type doping coupled to and between the first charge collecting region and the first plug, the first extension having a different doping concentration than the first charge collecting region; and

a second extension with n+ type doping coupled to and between the second charge collecting region and the second plug, the second extension having a different doping concentration than the second charge collecting region.

2. (Cancelled)

3. (Previously Presented) The pixel of claim 1 wherein the first and second extensions are configured to operate such that they are not fully depleted of mobile charge.

4-21. (Cancelled)

22. (Previously Presented) The pixel of claim 1 further including:

a first reset transistor having a source electrically coupled to the first n+ type doped plug, a drain coupled to a reference voltage, and a gate coupled to a reset signal line; and

a second reset transistor having a source electrically coupled to the second n+ type doped plug, a drain coupled to a reference voltage, and a gate coupled to a reset signal line.

23. (Previously Presented) The pixel of claim 1 further including:

a first amplifier transistor electrically coupled to the first n+ type doped plug, the first amplifier transistor having an output coupled to a first output node; and

a second amplifier transistor electrically coupled to the second n+ type doped plug, the second amplifier transistor having an output coupled to a second output node.

24. (Previously Presented) The pixel of claim 23, wherein:

the first amplifier transistor is a source follower amplifier having a gate coupled to the first n+ type doped plug, a drain coupled to a supply potential, and a source coupled the first output node; and

the second amplifier transistor is a source follower amplifier having a gate coupled to the second n+ type doped plug, a drain coupled to a supply potential, and a source coupled the second output node.

25. (Previously Presented) The pixel of claim 1, further including:

a third doped charge collecting region formed within the p type doped region and vertically separated from the first charge collecting region by the p type doped region, the third doped charge collecting region separated from an upper surface of the p type doped region by a p+ type surface region; and

a third n+ type doped plug extending from near the surface of the image sensor to the third charge collecting region.

26. (Previously Presented) The pixel sensor of claim 25, further including:

a first reset transistor having a source electrically coupled to the first n+ type doped plug, a drain coupled to a reference voltage, and a gate coupled to a reset signal line;

a second reset transistor having a source electrically coupled to the second n+ type doped plug, a drain coupled to a reference voltage, and a gate coupled to a reset signal line; and

a third reset transistor having a source electrically coupled to the third n+ type doped plug, a drain coupled to a reference voltage, and a gate coupled to a reset signal line

27. (Previously Presented) The pixel of claim 25 further including:

a first amplifier transistor electrically coupled to the first n+ type doped plug, the first amplifier transistor having an output coupled to a first output node;

a second amplifier transistor electrically coupled to the second n+ type doped plug, the second amplifier transistor having an output coupled to a second output node;

a third amplifier transistor electrically coupled to the third n+ type doped plug, the third amplifier transistor having an output coupled to a third output node.

28. (Previously Presented) The pixel of claim 27, wherein:

the first amplifier transistor is a source follower amplifier having a gate coupled to the first n+ type doped plug, a drain coupled to a supply potential, and a source coupled the first output node;

the second amplifier transistor is a source follower amplifier having a gate coupled to the second n+ type doped plug, a drain coupled to a supply potential, and a source coupled the second output node; and

the third amplifier transistor is a source follower amplifier having a gate coupled to the third n+ type doped plug, a drain coupled to a supply potential, and a source coupled the third output node